	Application No.	Applicant(s)
Office Action Summary	09/977,338	KAMIHARA, YOSHIYUKI
	Examiner	Art Unit
	LEILA MALEK	2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>17 January 2008</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1,4,5,8-17,19,20,22,23,25,26,28,29,31,32,34,35 and 37-40</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1,4,5,8-17,19,20,22,23,25,26,28,29,31,32,34,35 and 37-40</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>16 October 2001</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☒ All   b) ☐ Some * c) ☐ None of:

      1. ☒ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments with respect to claims 1 and 10 have been considered but

are moot in view of the new ground(s) of rejection.

Double Patenting

2.   The nonstatutory double patenting rejection is based on a judicially created
doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the
unjustified or improper timewise extension of the "right to exclude" granted by a patent
and to prevent possible harassment by multiple assignees.   A nonstatutory
obviousness-type double patenting rejection is appropriate where the conflicting claims
are not identical, but at least one examined application claim is not patentably distinct
from the reference claim(s) because the examined application claim is either anticipated
by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140
F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29
USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.
1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422
F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163
USPQ 644 (CCPA 1969).
        A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d)
may be used to overcome an actual or provisional rejection based on a nonstatutory
double patenting ground provided the conflicting application or patent either is shown to
be commonly owned with this application, or claims an invention made as a result of
activities undertaken within the scope of a joint research agreement.
        Effective January 1, 1994, a registered attorney or agent of record may sign a
terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with
37 CFR 3.73(b).

        Claims 1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35, 37-40 are rejected

on the ground of nonstatutory obviousness-type double patenting as being unpatentable

over claims 15-18 and 21-24 of U.S. Patent No. 6,990,597 in view of Takashi et al.

(hereafter, referred as Takashi) (US 5,553,104). Although the conflicting claims are not

identical, they are not patentably distinct from each other because: Applicants in claims

1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35, 37-40 of the instant

application recite all the limitations of claims 15-18 and 21-24 of the US 6,990,597,

except that the clock generation circuit includes an oscillation circuit. However, Takashi,

in the same field of endeavor, shows (see Fig. 1) a clock generation circuit comprising a

Voltage Control Oscillator (VCO) 14 that generates a timing clock 106. It would have

been obvious to one of ordinary skill in the art at the time of invention to include an

oscillator in the clock generation circuitry to generate the desired clock signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1, 4, 5, and 8-15 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Hirota et al. (hereafter, referred as Hirota) (US 6,567,484), Tanabe et

al. (hereafter, referred as Tanabe) (US 4,672,639), and Bazes (US 4,975,702), further in

view of Takashi et al. (hereafter, referred as Takashi) (US 5,553,104).

As to claim 1, Hirota discloses an apparatus comprising: an edge detection circuit

(see Fig. 4, 23-2) detecting between which two clock edges a data edge is located (see

Fig. 5 and column 3, lines 9-30), the two edges being among edges of first to N-th

clocks having the same frequency but mutually different phases (see the abstract and

column 2, lines 21-29); and a clock selection circuit which selects one clock (i.e. clock

#7) from among the first to N-th clocks (see column 3, lines 28-30), based on detection

information from the edge detection circuit. Hirota does not disclose that the selected

clock has been used as a sampling clock. Tanabe, in the same field of endeavor,

discloses a sampling pulse generator, which receives a plurality of clock signals having

the same frequency and phase differences (see the abstract). Tanabe further discloses

an additional signal (interpreted as data signal) is also inputted to the edge detector

(see Fig. 1), wherein phase relationship data are constructed and assembled and an

optimum one of the clock signals is selected and outputted based on the phase data as

the recovered sampling clock (see the abstract and column 3, lines 30-45, and see

column 1, lines 10-16). It would have been obvious to one of ordinary skill in the art at

the time of invention to use the optimum clock selected from a plurality of clocks (i.e. the

clock which samples the data in the middle) as the sampling clock, in order to sample

the data correctly and therefore more accurately recognize the incoming data (see

column 1, lines 62 to column 2, line 9). Tanabe further discloses that the edge

detection circuit comprises: a first holding circuit (see Fig. 3, e.g. 310) which holds data

(CRS interpreted as data) by using the first clock (CK0), . . . a J-th holding circuit (see

Fig. 3, e.g. 314), which holds data by using a J-th clock (CK4), . . . and an N-th holding

circuit (see Fig. 3, e.g. 317) which holds data by using the N-th clock (CK7); and a first

detection circuit (e.g. AN0) which detects whether or not there is a data edge between

the edges of the first clock and a second clock, based on data held in the first holding

circuit and a second holding circuit, . . . a J-th detection circuit (e.g. AN4) which detects

whether or not there is a data edge between the edges of the J-th clock (CK4) and a

(J+1)-th clock (CK5), based on data held in the J-th holding circuit (314) and a (J+1)-th

holding circuit (315), . . . and an N-th detection circuit (AN7) which detects whether or

not there is a data edge between the edges of the N-th clock (CK7) and the first clock

(CK0), based on data held in the N-th (317) and first (310) holding circuits, and wherein

the clock selection circuit 35 selects a clock from among the first to N-th clocks, based

on edge detection information from the first to N-th detection circuits, and outputs the

selected clock as the sampling clock. It would have been obvious to one of ordinary skill

in the art at the time of invention to modify Hirota as suggested by Tanabe to accurately

determine the edge of the data (see column 4, lines 10-24) and find the optimum

sampling clock. Hirota and Tanabe are silent in disclosing that there is a set-up time and

a holding time associated with first to N-th holding circuits. Bazes discloses that there is

a specified setup time, t_s and hold time t_h, for any clocked device (see column 5, lines

18-35). Bazes discloses that the setup time requirement of the flip-flop is met if the

signal has stable for at least the setup time before the next transition of the SDL tap,

and similarly, the hold time requirement of the flip-flop is met if the signal has been

stable for at least the hold time after the transition of the SDL tap (see column 5, lines

18-35). Bazes further discloses that the interval between each SDL output transition is

given by T_r/N, where T_r is the reference clock period and N is the number of SDL taps

(interpreted as the number of clock signals) (see column 4, last paragraph and column

6, first paragraph). Therefore inherently Tr/N (i.e., the interval between each SDL

transition) must be equal or greater than $(t_s + t_h)$, to meet the above requirements.

Hence $N \leq [T/(T_s+T_h)]$. It would have been obvious to one of ordinary skill in the art at

the time of invention to modify Hirota and Tanabe as suggested by Bazes to accurately

determine the location of the transitions in the digitized waveform (see column 6, first

paragraph). Hirota, Tanabe, and Bazes disclose all the subject matters claimed in claim

1, except that the clock generation circuit includes an oscillation circuit and generates

first to N-th clocks, wherein the oscillation circuit comprising: inversion circuits that are

connected serially; and buffer circuits, an output of each of the inversion circuits being

connected to an input of a corresponding buffer circuit among the buffer circuits, an

output of a final-stage inversion circuit among the inversion circuits being connected to

an input of an initial-stage inversion circuit among the inversion circuits via a feedback

line, the inversion circuits being disposed along a first line that is parallel to the

feedback line, the buffer circuits being disposed along a second line that is parallel to

the feedback line. Takashi, in the same field of endeavor, discloses a clock generation

circuit that includes an oscillation circuit 14 (see Fig. 1), and generates first to N-th

clocks, wherein the oscillation circuit comprising: inversion circuits (see Fig. 18 and

column 8, lines 15-22) that are connected serially; and buffer circuits (Bfr1-Bfr5), an

output of each of the inversion circuits being connected to an input of a corresponding

buffer circuit among the buffer circuits, an output of a final-stage inversion circuit among

the inversion circuits being connected to an input of an initial-stage inversion circuit

among the inversion circuits via a feedback line, the inversion circuits being disposed

along a first line that is parallel to the feedback line, the buffer circuits being disposed

along a second line that is parallel to the feedback line. It would have been obvious to

one of ordinary skill in the art at the time of invention to modify Hirota, Tanabe, and

Bazes as suggested by Takashi to provide a stable operation for clock generation and

recovery (see column 5, last paragraph).

As to claim 4, Bazes discloses that the number of clocks N is such that

$N=[T/(T_s+T_h)]$ (see rejection of claim 1).

As to claim 5, Hirota, Tanabe, Bazes, and Takashi disclose all the subject

matters claimed in claim 1, except that the number of clocks N of the first to N-th clocks

is such that N=5. However, since Applicant does not disclose any advantage for using 5

clocks in the system, therefore, it is a matter of design choice to sample the signal with

5 clocks and it would have been obvious to one of ordinary skill in the art at the time of

invention to use 5 clocks in the system to sample the signal to meet the system

requirements.

As to claim 8, Hirota discloses that the clock selection circuit selects from the first

to N-th clocks a clock having an edge that is shifted by a given set number M (e. g. 3 to

obtain clock #7) of edges from a data edge (see Fig. 5).

As to claim 9, Hirota, Tanabe, Bazes, and Takashi are silent in disclosing that the

number M is set to a number that ensures a set-up time and a hold time of a circuit

which holds data based on the generated sampling clock. However, it would have been

obvious to select the optimal clock in a place that ensures a set-up time and a hold time

of a circuit, which holds data based on the generated sampling clock to accurately

determine the location of the transitions in the digitized waveform (see column 6, first

paragraph).

As to claim 10, Hirota discloses an apparatus comprising: an edge detection

circuit (see Fig. 4, 23-2) detecting between which two clock edges a data edge is

located (see Fig. 5 and column 3, lines 9-30), the two edges being among edges of first

to N-th clocks having the same frequency but mutually different phases (see the

abstract and column 2, lines 21-29); and a clock selection circuit which selects one

clock (i.e. clock #7) from among the first to N-th clocks (see column 3, lines 28-30),

based on detection information from the edge detection circuit. Hirota discloses all the

subject matters claimed in claim 10, except that the selected clock has been used as a

sampling clock. Tanabe, in the same field of endeavor, discloses a sampling pulse

generator, which receives a plurality of clock signals having the same frequency and

phase differences. Tanabe further discloses an additional signal (interpreted as data

signal) is also inputted to the edge detector (see Fig. 1), wherein phase relationship

data are constructed and assembled and an optimum one of the clock signals is

selected and outputted based on the phase data as the recovered sampling signal (see

the abstract and column 3, lines 30-45, and see column 1, lines 10-16). It would have

been obvious to one of ordinary skill in the art at the time of invention to use the

optimum clock selected from a plurality of clocks (i.e. the clock which samples the data

in the middle) as the sampling clock, in order to sample the data correctly and therefore

more accurately recognize the incoming data (see column 1, lines 62 to column 2, line

9). Tanabe further discloses that the edge detection circuit comprises: a first holding

circuit (see Fig. 3, e.g. 310) which holds data (CRS interpreted as data) by using the

first clock (CK0), . . . a J-th holding circuit (see Fig. 3, e.g. 314), which holds data by

using a J-th clock (CK4), . . . and an N-th holding circuit (see Fig. 3, e.g. 317) which

holds data by using the N-th clock (CK7). It would have been obvious to one of ordinary

skill in the art at the time of invention to modify Hirota as suggested by Tanabe to

accurately determine the edge of the data (see column 4, lines 10-24) and find the

optimum sampling clock. As to the last limitation of claim 10, Hirota and Tanabe are

silent in disclosing that there is a set-up time and a holding time associated with first to

N-th holding circuits. Bazes discloses that there is a specified setup time, t_s and hold

time t_h, for any clocked device (see column 5, lines 18-35). Bazes discloses that the

setup time requirement of the flip-flop is met if the signal has stable for at least the setup

time before the next transition of the SDL tap, and similarly, the hold time requirement of

the flip-flop is met if the signal has been stable for at least the hold time after the

transition of the SDL tap (see column 5, lines 18-35). Bazes further discloses that the

interval between each SDL output transition is given by T_r/N, where T_r is the reference

clock period and N is the number of SDL taps (interpreted as the number of clock

signals) (see column 4, last paragraph and column 6, first paragraph). Therefore

inherently Tr/N (i.e., the interval between each SDL transition) must be equal or greater

than (t_s + t_h), to meet the above requirements. Hence $N \leq [T/(T_s+T_h)]$. It would have

been obvious to one of ordinary skill in the art at the time of invention to modify Hirota

and Tanabe as suggested by Bazes to accurately determine the location of the

transitions in the digitized waveform (see column 6, first paragraph). Hirota, Tanabe,

and Bazes disclose all the subject matters claimed in claim 10, except that the clock

generation circuit includes an oscillation circuit and generates first to N-th clocks,

wherein the oscillation circuit comprising: inversion circuits that are connected serially;

and buffer circuits, an output of each of the inversion circuits being connected to an

input of a corresponding buffer circuit among the buffer circuits, an output of a final-

stage inversion circuit among the inversion circuits being connected to an input of an

initial-stage inversion circuit among the inversion circuits via a feedback line, the

inversion circuits being disposed along a first line that is parallel to the feedback line,

the buffer circuits being disposed along a second line that is parallel to the feedback

line. Takashi, in the same field of endeavor, discloses a clock generation circuit that

includes an oscillation circuit 14 (see Fig. 1), and generates first to N-th clocks, wherein

the oscillation circuit comprising: inversion circuits (see Fig. 18 and column 8, lines 15-

22) that are connected serially; and buffer circuits (Bfr1-Bfr5), an output of each of the

inversion circuits being connected to an input of a corresponding buffer circuit among

the buffer circuits, an output of a final-stage inversion circuit among the inversion

circuits being connected to an input of an initial-stage inversion circuit among the

inversion circuits via a feedback line, the inversion circuits being disposed along a first

line that is parallel to the feedback line, the buffer circuits being disposed along a

second line that is parallel to the feedback line. It would have been obvious to one of

ordinary skill in the art at the time of invention to modify Hirota, Tanabe, and Bazes as

suggested by Takashi to provide a stable operation for clock generation and recovery

(see column 5, last paragraph).

As to claim 11, Bazes discloses that the number of clocks N is such that

$N=[T/(T_s+T_h)]$ (see rejection of claim 10).

As to claims 12 and 13, Hirota, Tanabe, Bazes, and Takashi disclose all the

subject matters claimed in claim 10 and 11, except that the number of clocks N of the

first to N-th clocks is such that N=5. However, since Applicant does not disclose any

advantage for using 5 clocks in the system therefore, it is a matter of design choice to

sample the signal with 5 clocks and it would have been obvious to one of ordinary skill

in the art at the time of invention to use 5 clocks in the system to sample the signal to

meet the system requirements.

As to claim 14, Hirota discloses that the clock selection circuit selects from the

first to N-th clocks a clock having an edge that is shifted by a given set number M (e. g.

3 to obtain clock #7) of edges from a data edge (see Fig. 5).

As to claim 15, Hirota, Tanabe, Bazes, and Takashi are silent in disclosing that

the number M is set to a number that ensures a set-up time and a hold time of a circuit

which holds data based on the generated sampling clock. However, it would have been

obvious to select the optimal clock in a place that ensures a set-up time and a hold

time of a circuit, which holds data based on the generated sampling clock to accurately

determine the location of the transitions in the digitized waveform (see column 6, first

paragraph).

4.   Claims 16, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Hirota, Tanabe, Bazes, and Takashi further in view of Yamauchi et

al. (hereafter, referred as Yamauchi) (US 5,517,155).

As to claims 16 and 17, Hirota, Tanabe, Bazes, and Takashi disclose all the

subject matters claimed in claims 1 and 10, except that sampling clock generation

circuit, further comprises: a PLL circuit having an oscillation circuit with a variably-

controlled oscillation frequency, and phase-synchronizing a clock generated by the

oscillation circuit with a base clock, wherein the first to N-th clocks is generated based

on outputs of first to N-th inversion circuits of an odd number of stages included in the

oscillation circuit. Yamauchi, in the same field of endeavor, discloses a PLL circuit (see

Fig. 2) having an oscillation circuit (block 6) with a variably-controlled oscillation

frequency, and phase-synchronizing a clock generated by the oscillation circuit with a

base clock (see column 6, last paragraph and column 7, first paragraph), wherein the

first to N-th clocks is generated based on outputs of first to N-th inversion circuits of an

odd number of stages included in the oscillation circuit (see Fig. 7, column 22,

paragraphs 2-3 and column 23, last paragraph). It would have been obvious to one of

ordinary skill in the art at the time of invention to modify Hirota, Tanabe, Bazes, and

Takashi as suggested by Yamauchi to accurately find the optimal clock synchronized

with the clock of the transmitter suitable for sampling the incoming data signal.

As to claims 19 and 20, Yamauchi further discloses that at least one of a

disposition of the first to N-th inversion circuits and interconnection of output lines of

the first to N-th inversion circuits is performed in such a manner that phase differences

between the first to N-th clocks are equal (see column 23, last paragraph).

5.   Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Hirota, Tanabe, Bazes, Talashi, and Yamauchi, further in view of Wendelrup (US

5,796,360).

As to claims 22 and 23, Hirota, Tanabe, Bazes, Takashi, and Yamauchi are silent

in discloseing that the lines for the first to N-th clocks are interconnected in such a

manner that the parasitic capacitances of lines of the first to N-th clocks are equal.

Wendelrup, in the same field of endeavor discloses a controlled clock generator (see

column 1, lines 8 and 9). Wendelrup further discloses that in a design for

implementation on a CMOS integrated circuit, one must ensure that all of the output

nodes of the logic circuitry 907 have equal parasitic capacitances (see column 7, last

paragraph and Fig. 9). It would have been obvious to one of ordinary skill in the art at

the time of invention to Modify Hirota, Tanabe, Bazes, Takashi, and Yamauchi as

suggested by Wendelrup in order to have uniform delays introduced for each of the

phase clocks (see column 7, last paragraph).

6.   Claims 25, 26, 31, and 32 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Hirota, Tanabe, Bazes, and Takashi further in view of Fujimori et al.

(hereafter, referred as Fujimori) (US 6,477,181).

As to claim 25, Hirota, Tanabe, Bazes, and Takashi disclose all the subject

matters claimed in claim 25 (for the sampling clock generation circuit see the rejection

of claim 1) except for a circuit that holds data, based on the sampling clock generated

by the sampling clock generation circuit, and performs given processing for data

transfer, based on the held data. Fujimori discloses a data communication apparatus

(see Fig. 6) comprising a sampling clock generator 42 and a sound I/O 41 which writes

the audio data into its internal output FIFO buffer and then reads out the data from the

output FIFO buffer in accordance with the sampling pulses to transfer the read-out data

to the DAC for digital-to-analog conversion (see column 6, last paragraph). It would

have been obvious to one of ordinary skill in the art at the time of invention to modify

Hirota, Tanabe, Bazes, and Takashi as suggested by Fujimori to improve the data

communication system (see column 27, lines 16-25).

As to claim 26, Hirota, Tanabe, Bazes, and Takashi, disclose all the subject matters claimed in claim 26 (for the sampling clock generation circuit see the rejection of claim 10) except for a circuit which holds data, based on the sampling clock generated by the sampling clock generation circuit, and performs given processing for data transfer, based on the held data. Fujimori discloses a data communication apparatus (See Fig. 6) comprising a sampling clock generator 42 and a sound I/O 41 which writes the audio data into its internal output FIFO buffer and then reads out the data from the output FIFO buffer in accordance with the sampling pulses to transfer the read-out data to the DAC for digital-to-analog conversion (see column 6, last paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Hirota, Tanabe, Bazes, and Takashi as suggested by Fujimori to improve the data communication system (see column 27, lines 16-25).

As to claims 31 and 32, Fujimori further shows a device, which performs storage processing (see Fig. 6, 31-33) on data transferred through the data transfer control device (see Fig. 6, 41 and 42) and the bus 44.

7.   Claims 28, 29, 34, and 35, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirota, Tanabe, Bazes, Takashi, and Fujimori, further in view of Applicant's admitted prior art (Applicant's background of invention).

As to claims 28 and 29, Fujimori discloses that the data has been transferred by using bus 44 in the system (see Fig. 6). However, Fujimori does not disclose data transfer is in accordance with the Universal Serial Bus (USB) standard. Applicant in the background of invention discloses that the USB standard has the advantage of

enabling the use of connectors of the same standard to connect peripheral equipment
such as a mouse, keyboard, and printer, which are connected by connectors of
different standards, and of making it possible to implement plug-and –play and hot-plug
features (see page 1). Therefore, it would have been obvious to one of ordinary skill in
the art at the time of invention to use the USB standard for the reasons stated above.

As to claims 34 and 35, Fujimori further shows a device, which performs storage
processing (see Fig. 6, 31-33) on data transferred through the data transfer control
device (see Fig. 6, 41 and 42) and the bus 44.

Allowable Subject Matter

8.   Claims 37-40 are objected to as being dependent upon a rejected base claim,
but would be allowable if rewritten in independent form including all of the limitations of
the base claim and any intervening claims.

Conclusion

9.   Applicant's amendment necessitated the new ground(s) of rejection presented in
this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP
§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37
CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE
MONTHS from the mailing date of this action. In the event a first reply is filed within
TWO MONTHS of the mailing date of this final action and the advisory action is not
mailed until after the end of the THREE-MONTH shortened statutory period, then the
shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Leila Malek whose telephone number is 571-272-8731.

The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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